CONTROL DATA
CORPORATION

CONTROL DATA®
CYBER 170 COMPUTER SYSTEM
7030-1XX EXTENDED CORE STORAGE SUBSYSTEM

HARDWARE REFERENCE MANUAL

REVISION RECORD

REVISION	DESCRIPTION
A	Manual released.
(10-1-74)	

Publication No.
60430000

Address comments concerning this manual to:

Control Data Corporation
Technical Publications Department
4201 North Lexington Avenue
Arden Hills, Minnesota 55112

or use Comment Sheet in the back of this manual.

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SYSTEM DESCRIPTION 1

INTRODUCTION

The CONTROL DATA® CYBER 170 Extended Core Storage (ECS) Subsystem is an on-line, semirandom access, magnetic core memory system which augments central memory. It is a fixed-word-length system, and is capable of two-way communication.

SYSTEM CONFIGURATION

The ECS subsystem consists of core storage, an ECS controller, and a distributive data path. An ECS coupler interfaces the ECS system with the central computer system. The ECS coupler is part of the mainframe. Figure 1-1 shows an ECS system configuration.

Extended core storage consists of 1, 2, 4, 8, or 16 memory banks, each capable of storing 131,072 60-bit words. A cabinet (called a bay) holds up to four memory banks. Each ECS bank address stores one ECS record. An ECS record contains eight words, each consisting of 60 data bits plus one parity bit. Assembly/disassembly of 60/480-bit words during data transfers is performed in the ECS banks. References as low as one 60-bit word are possible. Extended core storage is capable of a maximum data transfer rate of one 60-bit word per 100 nanoseconds.

The ECS controller regulates access to the ECS banks. The controller has four access channels and four ECS interfaces. Each access channel connects to one ECS coupler or one distributive data path (interface units), and carries 60 data bits plus one parity bit. The controller performs time-sharing on the four access channels. Each of the four ECS interfaces carries 60 data bits plus one parity bit. Data parity is generated and checked on the access channels and ECS interfaces. The ECS controller also has:

- Address parity checking
- Flag register which software can use to coordinate ECS references
- Capability of switching 262K and larger systems to 50 percent of capacity

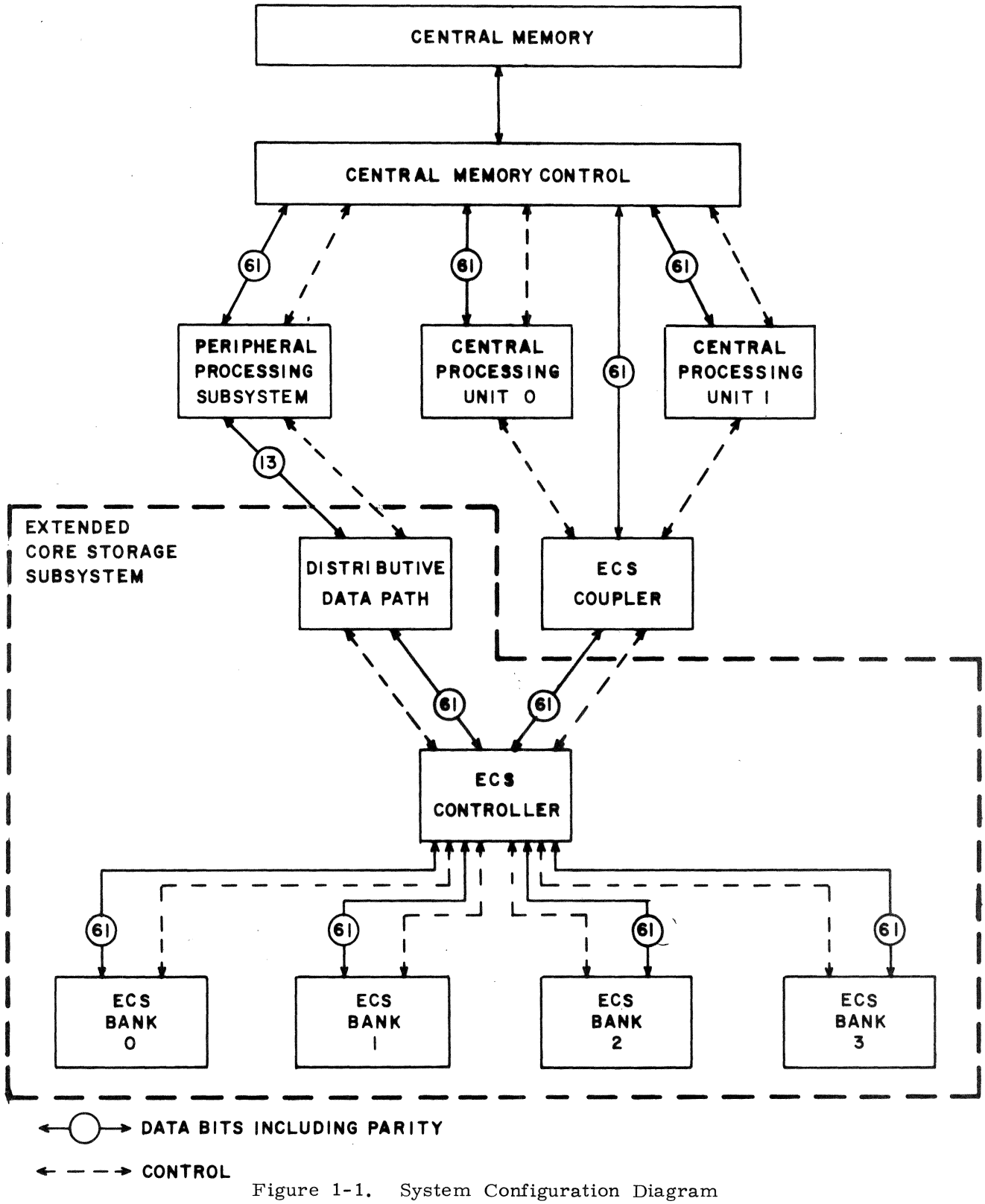


Figure 1-1. System Configuration Diagram

The distributive data path (DDP) provides a means for peripheral processors to communicate directly with ECS. The DDP is described in a separate section of this manual.

PRODUCT DEFINITIONS

CYBER 170 ECS Subsystems are available in several different capacities. Memory expansion kits increase the system storage capacity. Additional DDPs are also available. Product numbers for the expansion kits and DDPs are defined below. An ECS coupler must be installed on the mainframe in order for an ECS subsystem to function.

ECS Subsystems (Includes memory, an ECS controller, and a DDP)

Product Number	Memory Banks	Storage Capacity (60-bit words)
7030-101	1	131,072
7030-102	2	262,144
7030-104	4	524,288
7030-108	8	1048,576
7030-116	16	2097,152

ECS Memory Expansion Kits (Standard options)

Product Numbers	Storage Increase From	To
10319-1	131,072	262,144
10319-2	262,144	524,288
10319-4	524,288	1048,576
10319-8	1048,576	2097,152

The DDP product number is 6642-2. The standard DDP has one port.† Up to three additional ports can be installed. The additional ports are called DDP registers, and the product number is 10280-10.

† Refer to the DDP section of this manual.

DATA FORMAT

An ECS record consists of eight 60-bit words plus one parity bit for each word. Figure 1-2 illustrates the data format.

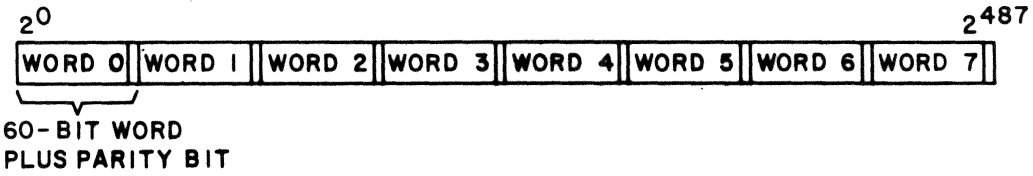


Figure 1-2. Data Format

CPU/ECS COMMUNICATIONS 2

INSTRUCTIONS

Two instructions reference ECS.

011jK BLOCK COPY (Bj) + K WORDS FROM ECS TO CENTRAL MEMORY

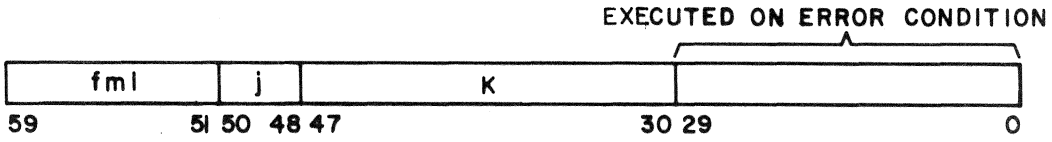


Figure 2-1. 30-Bit Read Instruction

Figure 2-1 shows a 30-bit instruction in which bits 30 through 47 are used as an operand K. This instruction reads a sequence of 60-bit words from consecutive addresses in ECS and copies them into a block of consecutive addresses in central memory. The block of words begins at address (X0) + RAE in ECS. The words are stored in central memory beginning at address (A0) + RAC.†

Addition of the integers (Bj) and K determines the number of 60-bit words transferred. Both the CPU and ECS check the result of the addition. If the CPU finds that bit 17 (the highest order bit) in the result is set, the result is treated as a negative block count and no transfer occurs. If the ECS coupler finds that the result is zero, no data transfers. In these cases, the instruction executes as a pass instruction and exits to P + 1.

The normal exit for this instruction is to P + 1. On an error condition, an exit to the lower 30 bits of the instruction word occurs. The lower 30 bits should contain a jump instruction to an error routine.

† Refer to the address formation section of this manual.

012jK BLOCK COPY (Bj) + K WORDS FROM CENTRAL MEMORY TO ECS

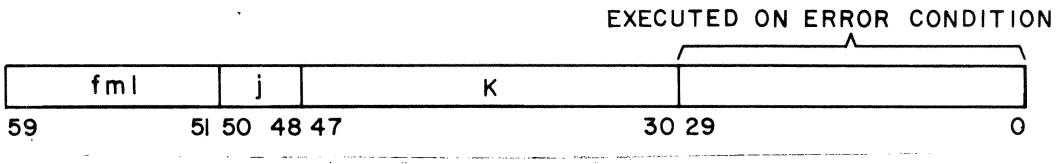


Figure 2-2. 30-Bit Write Instruction

Figure 2-2 shows a 30-bit instruction in which bits 30 through 47 are used as an operand K. This instruction reads a sequence of 60-bit words from consecutive addresses in central memory and copies them into a block of consecutive addresses in ECS. The block of words begins at address (A0) + RAC in central memory. The words are stored in ECS, beginning at address (X0) + RAE. †

Addition of the integers (Bj) and K determines the number of 60-bit words transferred. Both the CPU and ECS check the result of the addition. If the CPU finds that bit 17 (the highest order bit) in the result is set, the result is treated as a negative block count and no transfer occurs. If the ECS coupler finds that the result is zero, no data transfers. In these cases, the instruction executes as a pass instruction and exits to P + 1.

The normal exit for this instruction is to P + 1. On an error condition, an exit to the lower 30 bits of the instruction word occurs. The lower 30 bits should contain a jump instruction to an error routine.

The two ECS block copy instructions are intended to move data between central memory and ECS as fast as possible. With the exception of PPS requests, all other operation stops during these block transfers. PPS requests do not delay block transfers. All instructions issued prior to these instructions execute to completion. No further instructions are issued until these block transfers are finished.

These instructions are illegal if they are not in the upper 30 bits of the instruction word, or if the system does not have ECS. An attempt to execute will result in an exit to MA (monitor address) or a program stop. This exit occurs regardless of the exit mode bits in the exchange jump package. † †

† Refer to the address formation section of this manual.

†† For more information, refer to the Computer System Hardware Reference Manual (Publication Number 19981200 for CYBER 170, Models 172/173/174 and Publication Number 60420000 for CYBER 170, Model 175).

INSTRUCTION EXECUTION

An interface unit (ECS coupler or DDP) initiates an ECS reference by transmitting in parallel a request signal, a read/write signal, and a 24-bit address word plus one parity bit to an ECS controller access. The controller monitors the access channels sequentially, and responds to a requesting channel by sending an accept signal to the interface unit. The accept signal indicates that the controller is ready for the transfer of one ECS record. If the ECS memory bank is not available, the controller sends an abort signal 25 nanoseconds after the accept. Four conditions cause ECS to be unavailable:

1. The bank may be in maintenance mode.
2. The bank may have lost power.
3. The requested bank is not in the system.
4. The ECS controller has detected an address parity error. In this case, the controller does not send an accept signal to the interface unit.

The ECS controller allows one ECS record (eight 60-bit words) to transfer for each request. During a read ECS operation, the controller receives eight 60-bit words from ECS, and transmits them to an interface unit via an access channel. ECS data parity is checked, and data parity is transmitted on the access channels on a read ECS operation. On a write ECS operation, the controller receives eight 60-bit words via an access channel and transfers them to ECS. The access channel data parity is checked, and ECS data parity is generated for a write ECS operation. Assembly/disassembly of the 60/480-bit words during a read or write operation is done in the ECS banks. References as low as one 60-bit word are possible in the read ECS and write ECS modes.

ERROR RESPONSES

For the following error conditions, an exit to the lower 30 bits of the instruction word occurs. The lower 30 bits of the instruction word should contain a jump instruction to an error routine.

1. Data parity error in the 60-bit word received by the ECS controller during a write ECS operation. The controller transmits an ECS controller parity error signal to the ECS coupler, and stores the bad data into ECS with its incorrect parity. The exit to the lower 30 bits of the instruction word occurs after the transfer of the ECS record in which the bad data was detected.
2. Data parity error in the 60-bit word received by the ECS coupler during a read ECS operation. The coupler generates a parity error signal, and the bad data is allowed to transfer. The exit to the lower 30 bits of the instruction word occurs after the transfer of the ECS record in which the bad data was detected.
3. Data parity error between the ECS controller and ECS memory during a read ECS operation. The controller sends an ECS parity error signal to the ECS coupler, and the bad data is allowed to transfer. The exit to the lower 30 bits of the instruction word occurs after the transfer of the ECS record in which the bad data was detected.
4. Parity error in the address received by the ECS controller. When it detects an address parity error, the ECS controller does not transmit an accept signal. Instead, it sends an abort signal and an ECS controller parity error signal to the interface unit. The controller does not request ECS and no data transfers. An exit to the lower 30 bits of the instruction word occurs immediately.
5. The referenced ECS bank is in maintenance mode or has lost power. An exit to the lower 30 bits of the instruction word occurs immediately.
6. An attempt to reference a nonexistant address. On an attempted write operation, no data transfers and an exit to the lower 30 bits of the instruction word occurs immediately. If the attempted operation is a read, zeros transfer to central memory; this is a method of clearing blocks of central memory.

Each access channel has a switch which disables address and data parity for that channel.

TIMING

Timing during ECS communications consists of the access time between the ECS controller and the ECS memory banks, and delays due to concurrent requests in the access channels.

A system must have four or more 131K memory banks in order to achieve a transfer rate of one 60-bit word per 100 nanoseconds. If a system has four or more banks, the ECS controller staggers ECS references so that one bank is referenced while the previously referenced bank is recovering, and so on. If ECS has two 131K memory banks, the ECS controller allows two sequential requests. A third request must wait until a bank becomes free. Thus, 60-bit words transfer in a pattern of one word per 100 nanoseconds for 1600 nanoseconds, wait 1600 nanoseconds, transfer another 16 words, and so on. This gives an effective rate of one word per 200 nanoseconds. If the system has one 131K bank, the ECS controller allows a second request only after the first memory cycle is complete. Sixty-bit words transfer in a pattern of eight words per 100 nanoseconds for 800 nanoseconds, wait 2400 nanoseconds, and so on. The effective transfer rate is one word per 400 nanoseconds.

When it is doing a block transfer operation, an ECS coupler must request the ECS controller every 800 nanoseconds in order to maintain the maximum rate of one 60-bit word per 100 nanoseconds. If other access channels are requesting concurrently, the coupler must wait until the other channels transfer one ECS record and time gaps occur during the block transfer. Use of the flag register to coordinate ECS communications minimizes concurrent requests. The flowchart in Figure 2-3 shows the timing for one ECS request. In using the flowchart to calculate transfer times, an uninterrupted block transfer incurs the access time only at the beginning of the transfer. Once the transfer is under way, the memory bank access time determines the transfer rate.

FLAG REGISTER

The controller has an 18-bit flag register to allow programs to provide information about the current or previous operations. One of its uses could be analogous to a reserved status word being maintained in ECS but available at far greater speed, since ECS references are not made. The register cannot be read directly; instead, an interface unit must interrogate it and/or write into it.

The flag register is selected by performing an ECS read or write operation with bit 23 set in the ECS address.† The operation is the same for either a read or write operation and is not affected by the 50 percent capacity reduction.

† Refer to the appropriate interface manual for flag register selection.

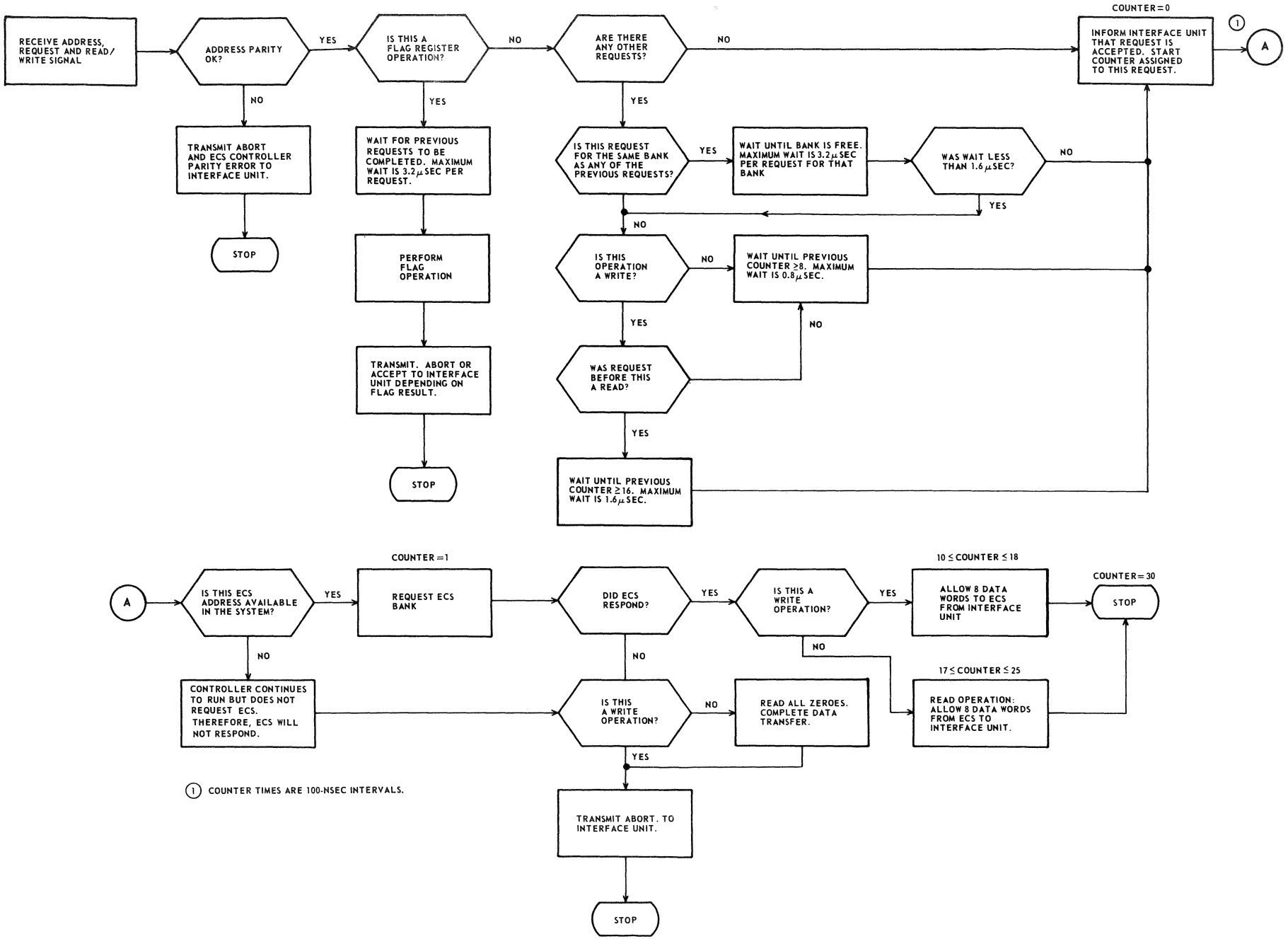


Figure 2-3. Controller Access Timing

The address is sent to the controller, as is any other ECS address. Since bit 23 is set, the controller recognizes this as a flag register operation. It then translates bits 22 and 21 to see what function is to be performed.

The controller responds to a flag register function by sending either an abort or an accept back to the interface unit.

For a flag register operation the ECS address is considered to have three parts plus one parity bit (Figure 2-4).

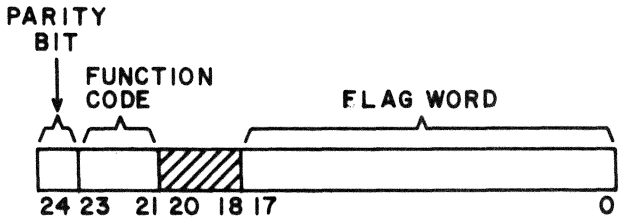


Figure 2-4. ECS Address Format for Flag Register Operation

1. Function code (N) is bits 21 through 23. Bit 23 is always set for a flag register operation.
2. Bits 18 through 20 are not used.
3. The flag word is bits 0 through 17. These bits are compared with or entered into the flag register, depending on the function specified by N.

If the ECS address sent to the controller during a flag register operation has bad parity, the controller does not send an accept signal to the interface unit. Instead, it sends an abort signal and an ECS controller parity error signal. The flag register does not change. An exit to the lower 30 bits of the instruction word occurs immediately.

FLAG FUNCTION CODES

Four operations can be specified by bits 21 and 22.

N=4; READY/SELECT

A bit by bit comparison is made between the contents of the flag register and the flag word. If all the set bits in the flag word are cleared in the flag register, a positive comparison has been made and all the set bits in flag word are entered into the flag register. The cleared bits in the flag word have no effect on the flag register.

Example: (Only three bits are shown)

Initial contents of flag register = 010
Flag word = 101

(This is a positive comparison so that flag register is changed and an accept is transmitted by the controller to the interface unit.)

Final contents of flag register = 111

If a positive comparison is not made, the flag register remains unchanged and an abort is transmitted to the interface unit.

Example: (Only three bits are shown)

Initial contents of flag register = 010
Flag word = 111

(This is a negative comparison so the flag register is unchanged and transmits an abort to the interface unit.)

Final contents of flag register = 010

N=5; SELECTIVE SET

No comparison is made. All set bits in the flag word are set in the flag register. The only response is an accept.

Example: (Only three bits are shown)

Initial contents of flag register = 010
Flag word = 100

Final contents of flag register = 110

N=6; STATUS

This is the same as a ready/select code, but the flag register is not changed on a positive comparison. The comparison is made in the same manner and the exit conditions are the same.

N=7; SELECTIVE CLEAR

No comparison is made. All set bits in the flag word are cleared in the flag register. The only response is an accept.

Example: (Only three bits are shown)

Initial contents of flag register = 110

Flag word = 101

Final contents of flag register = 010

USE OF THE FLAG REGISTER TO COORDINATE ECS TRANSFERS

Because of the inefficiency of allowing more than one interface unit to request ECS at the same time, the controller has a flag register available which can be used by the software to coordinate the ECS transfers. The following discussion demonstrates the advantages of using the flag register as a status register.

Assume that a transfer is underway. A second interface unit can perform a flag register operation on a pre-defined bit which may inform it that ECS is being used. This will delay the actual data transfer by only 300 nanoseconds minimum or by 3.5 microseconds in the worst case. If a second and third interface unit are also requesting flag register operations, the controller will perform them before returning to the data transfer. In this case, the second and third computers will add only 300 nanoseconds each to the original delay of 3.5 microseconds.

Assume that four 65K computers are using a 500K ECS system. Each computer wishes to transfer 5000 data words from ECS; that is, a total of 20,000 words. If all four are allowed to request ECS at the same time, the effective transfer rate as it appears to any one computer is one 60-bit word every 400 nanoseconds, even though ECS is running at full speed. Since there is a total of 20,000 words to be transferred, the total transfer time for all four computers is 2 milliseconds. This is the best case and ignores the conflicts due to requesting the same bank. In this example, bank conflicts could occur a significant percentage of the time. Therefore, the calculated transfer time of 2 milliseconds is less than the actual time required. Worst case transfer time is 400 nanoseconds multiplied by 20,000 words or 8 milliseconds.

Assume now that the transfers are sequential with one unit transferring data and the other three performing flag register operations to status ECS. These flag operations are done every 50 microseconds. The flag operations are not performed back to back, but instead, each one incurs an average penalty of 1.6 microsecond. The operation then takes 300 nanoseconds. This means that there is a total of 1.9-microsecond penalty for each flag operation.

Without an interruption the first unit would take 500 microseconds to transfer the data. However, each of the other units would interrupt the transfer ten times; a total of 30 in all. This would add 57 microseconds (30 by 1.9 microseconds) to the first 5000-word transfer, giving 557 microseconds. There will be only two units doing flag operations during the second 5000 words, one machine during the third 5000 words, and none during the last 5000 words. Therefore, the total transfer time will be:

(500 + 57) + (500 + 38) + (500 + 19) + (500) microseconds†

This gives a total of 2.114 milliseconds. This is only slightly more than the best case time and a considerable improvement over the worst case time of 8 milliseconds. The system's performance is further enhanced because the first computer can start using its data only 557 microseconds after starting a transfer. This is in marked contrast to the 2-milliseconds delay when the flag register is not used.

The flag register can be used to advantage for improving the total transfer rate of the ECS system, but it is particularly useful where priority transfers are necessary.

ADDRESSING

ECS has 1, 2, 3, 4, 8, or 16 banks of 131,072 words. Each ECS bank address stores one ECS record. One ECS record contains eight words each, consisting of 60 data bits plus one parity bit. References as low as one 60-bit word are possible.

FORMAT

A 25-bit word addresses ECS. Bit 2^{24} is for address parity. Bits 2^0, 2^1, and 2^2 indicate the 60-bit word within the ECS record. The format for bits 2^3 through 2^{19} varies with the memory size of the system. Figure 2-6 illustrates the address formats. Bits 2^{21}, 2^{22}, and 2^{23} are used during flag register operations. If an illegal address bit is set, it causes an exit to the lower 30 bits of the instruction word. The address format changes when the system is reduced to 50 percent of capacity.

† This ignores the initial access time.

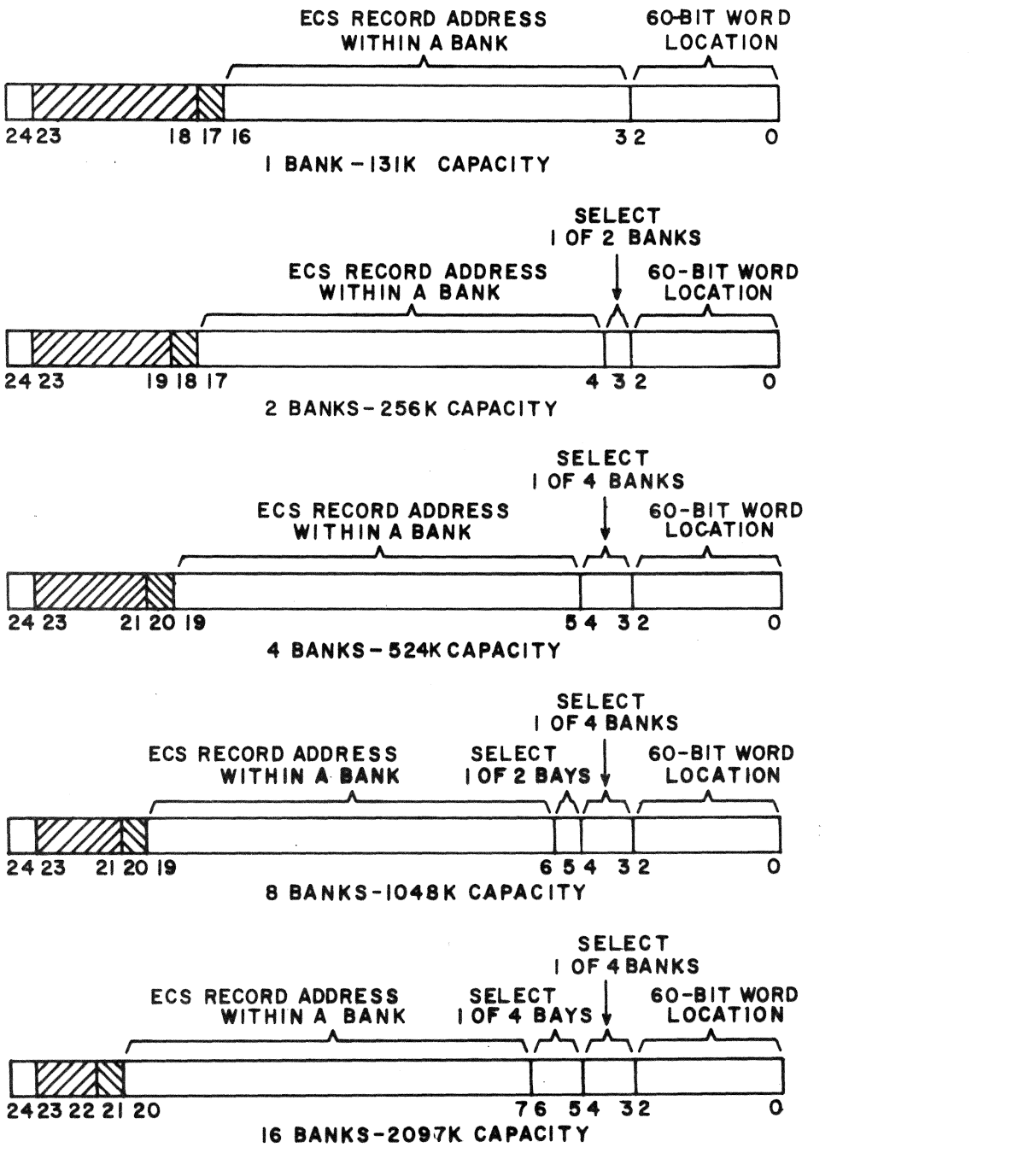


Figure 2-5. Address Formats

FORMATION

Initial addresses used during CPU/ECS communications automatically form, when the ECS instructions execute, by the addition of quantities contained in the exchange jump package.†

The initial ECS address, (X0) + RAE, forms by the addition of the quantity in the lower 24 bits of register X0 to RAE (the reference address for ECS). In the addition, both quantities are taken as positive with the upper 36 sign bits (zeros) extended. The initial address in central memory, (A0) + RAC, forms similarly. That is, the quantity in register A0 adds to RAC (the reference address for central memory). The lower six bits of RAE and RAC are always zero.

The program must place the relative addresses in A0 and X0 before the ECS instructions execute. The exchange jump package contains the reference addresses RAE and RAC. The exchange jump package also contains the field lengths for central memory and ECS (FLC and FLE).

RANGE FAULTS

The following three address range fault conditions can occur when the ECS instructions execute.

1. Word count fault.

   If, in forming the word count, (Bj) + K, the result is negative (bit 2^{17} in the result = 1), an address range fault occurs. If the address out of range bit is set in the exit mode register, an error stop occurs. If this bit is clear, the central processor passes to the next instruction word at (P) + 1 with no data transfer.

2. Central memory address out of range.

   Central memory address out of range is checked by comparing FLC with the sum, (A0) + (Bj) + K. FLC must be greater than this sum or an address range fault occurs. If the address out of range bit is set in the exit mode register, an error stop occurs. If this bit is clear, the central processor passes to the next instruction word at (P) + 1 with no data transfer.

† For more information, refer to the Computer System Hardware Reference Manual (Publication Number 19981200 for CYBER 170, Models 172/173/174 and Publication Number 60420000 for CYBER 170, Model 175).

3. ECS address out of range.

   Extended core storage address out of range is checked by comparing FLE with the sum, (X0) + (Bj) + K. In the comparison, FLE is a 24-bit quantity with 36 upper-order bits of sign extended; X0 holds the 24-bit address quantity with 36 zeros occupying the upper-order bit positions. The result of this subtraction should always be negative. If positive, an address range fault occurs. If the address out of range bit is set in the exit mode register, an error stop occurs.

   If this bit is clear, the central processor passes to the next instruction word at (P) + 1 with no data transfer.

Address range checks are made on the entire block of both extended core storage and central memory addresses before the transfer (read or write) is begun. If any address in the block to be transferred is out of range, either in central memory or extended core storage, no data is transferred, regardless of whether or not the address out of range bit is set in the exit mode register.

EXCHANGE JUMP DURING ECS COMMUNICATION

If an exchange jump occurs while an extended core storage transfer is in progress, the exchange waits until completion of a record. Operation is then as follows:

1. If the record just completed is the last record of the block transfer, and the transfer was error-free, the central processor exits to (P) + 1. The exchange jump then takes place.
2. If the record just completed is the last record of the block transfer and an error condition exists, the central processor exits to the lower instruction, executes it, and the exchange jump is performed.
3. If the record just completed does not complete the block transfer, the exchange jump occurs, and (P) are stored in the exchange jump package. A return exchange jump to this program begins execution with the ECS read or write instruction and restarts the transfer. The transfer does not resume at the point at which it was truncated; rather, the entire transfer must be repeated.

REDUCTION TO 50 PERCENT OF CAPACITY

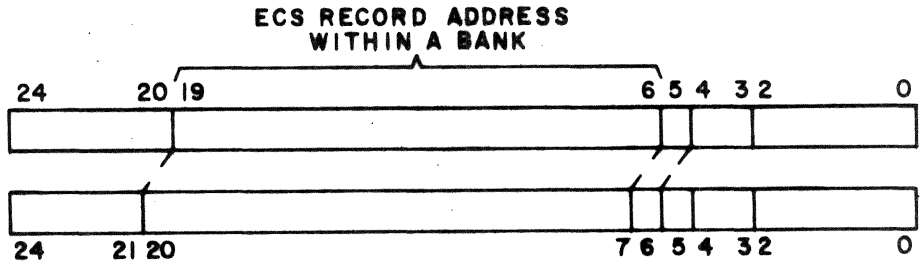
The system can be reduced to half of the configured capacity by a switch in the controller. This is done by left-shifting some address bits by one position (Table 2-1). This means that one of the bank selection bits in the controller address register is not used. This bit is set or cleared, depending on which half of the system is to be used. With the bit set, the upper half of the addresses are available. With the bit cleared, the lower half of the addresses are available. The selection is made by a second switch on the controller.

The capacity reduction is done per channel. It is therefore possible to degrade two channels and assign complementary halves of ECS to each channel. For example, in a 524K system, 262K could be assigned to channel 1 and the other 262K assigned to channel 2. The flag register operations are not affected by the capacity reduction.

TABLE 2-1. ADDRESS SHIFTING

Configuration	Bits Shifted		Selection Bit
	From:	To:	
262K	3-17	4-18	3
524K	4-18	5-19	4
1048K	5-19	6-20	5
2097K	6-20	7-21	6

Figure 2-6 shows an example of an address shifted by the 50 percent capacity reduction.



Bit 2^5 is set/cleared by switch on ECS controller.

Figure 2-6. Address Shift in a 1048K System

OPERATION IN ZERO PARITY MODE

The ECS coupler can check its parity network by requesting ECS data with the parity bit forced to zero. To do this, the coupler must transmit a one on the zero parity line every 100 nanoseconds for as long as zero parity is desired.

PPS/ECS COMMUNICATIONS 3

GENERAL DESCRIPTION

The DDP is a piece of hardware which makes two-way communication possible between ECS and any CDC CYBER 170 series PPS. The DDP contains one PPS interface, and is expandable up to three more identical interfaces. The PPS interfaces are called ports, and the additional interfaces may also be referred to as DDP registers (DDPR). Each port connects to one I/O channel. A scanner monitors the ports and sequentially connects requesting ports to the ECS controller. The DDP has one interface with one access of an ECS controller. Figure 3-1 shows the DDP/system configuration.

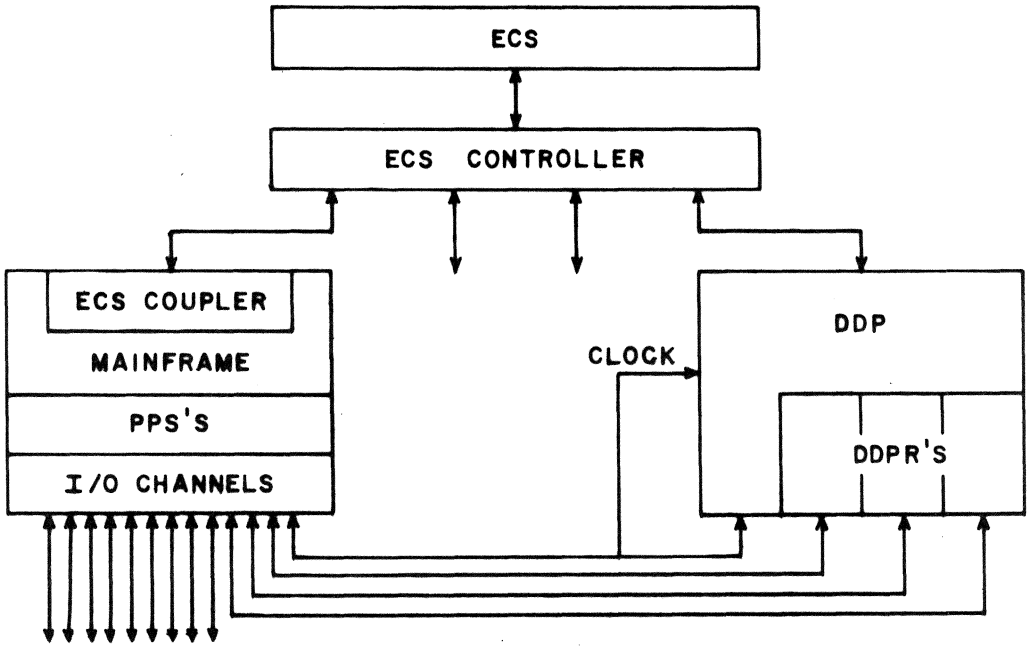


Figure 3-1. DDP/System Configuration

A PPS communicates with one port of a DDP through an I/O channel. Information transfers in words consisting of 12 data bits plus one parity bit. Between ECS and the DDP, information transfers in words of 60 data bits plus one parity bit. The DDP assembles 12-bit words into 60-bit words during a write operation and disassembles 60-bit words into 12-bit words during a read operation. The DDP allows block transfers

or references of as low as one 60-bit word. In addition to data, flag register communication is possible. Figure 3-2 illustrates the word format.

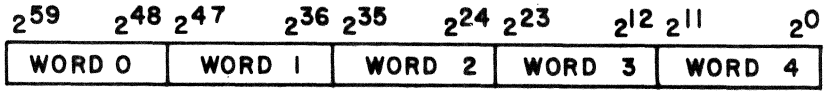


Figure 3-2. DDP Word Format

PROGRAMMING THE DDP

Twelve-bit function codes transmitted by a PPS on an I/O channel control the DDP. The upper three bits of the function code are the equipment select code (5). The remaining nine bits designate which function the DDP will perform. The PPS transmits function codes on an inactive channel. The DDP responds to valid function codes by transmitting an inactive signal to the I/O channel. Table 3-1 lists the DDP function codes.

TABLE 3-1. DDP FUNCTION CODES

Function	Code
Block Read ECS	5X01
Read ECS, 1 Reference	5X41
Function Flag Register (Bit 2^{23} of the address register must be set.)	5X01
Write ECS	5Y02
Select Status	5Z04
Master Clear Port	5010
Maintenance Mode Read	5Z21
Maintenance Mode Write	5022

NOTE

Normal Operation	X, Y, or Z = 0
Invert Channel Parity	X or Z = 1
Function ECS Controller to Send Zero Parity with Data	X = 2
Send Zero Parity to ECS Controller with Data	Y = 2
Send Zero Parity to ECS Controller with Address	X or Y = 4

The DDP responds to all function codes with the correct equipment select code and parity. When parity checking is disabled, the DDP responds to all function codes with the proper equipment select code. Appendix A contains DDP programming examples.

BLOCK READ ECS - 5X01

The read ECS function has three modes called block read, read 1 reference, and function flag register.

The block read ECS mode causes data to transfer from ECS to the PPS. The DDP responds to a read ECS function by inactivating the I/O channel to which it is connected. The PPS must then activate the I/O channel before it transmits two 12-bit words to the DDP. These two words designate the address from which the first 60-bit ECS word will be read. The DDP loads the two words into a 24-bit address register. The first word loads into the upper 12 bits, and the second word loads into the lower 12 bits.

During a block read ECS operation, the DDP accumulates eight 60-bit words (one ECS record). Each time an ECS record becomes available, the DDP disassembles it into 12-bit words and transmits them to the PPS. At the same time, it accumulates the next ECS record. The address register automatically increments for each 60-bit word read out of ECS. Unless an error condition occurs, data transfers in this way until the PPS inactivates the I/O channel to which the DDP is connected.

The following four error conditions will cause the DDP to terminate a block read operation.

- I/O Channel Parity Error
- ECS Controller Parity Error
- ECS Parity Error
- ECS Abort

If it detects channel parity error in the two address words from the PPS, the DDP will inactivate the I/O channel. The DDP responds to an ECS error condition by inactivating the requesting I/O channel after the previous ECS reference transfers to the PPS. The DDP transmits the inactive signal on an empty channel rather than full. This allows the PPS to determine whether or not the DDP will send an inactive. If the channel is full, The PPS can send an inactive without risking a hang-up. If the channel is empty, the PPS generated inactivate is illegal on the basis that the DDP may disconnect.† When the PPS inactivates an I/O channel, the status word must be read to determine the reason for the inactivate. In the case of parity error, issuing a maintenance mode read function (5021) will cause the PPS to transmit up to 16 60-bit ECS words stored in the PPS buffer register. After the buffer register empties, a new read ECS function and address must be issued to read more data.

The following is an instruction sequence to do a block read ECS.

```
      FCN     5001    Send read function
      ACN             Activate channel
      LDN        2
      OAM     XXXX    Output two words of address
      IJM        D    Check for inactive, in case of abort or parity error
      LDC     XXXX    Load input word count
      IAM     XXXX    Input
F     IJM        D    If inactive, then the channel was inactivated by the
                       DDP, read status
      EJM        F    Wait for change from active and empty state before
                       inactivating channel
      DCN
E     XXX             Continuation of program
D     XXX             Read status, proceed to error check routine
```

† If software uses the unhangable channel feature, the PPS may safely inactivate the I/O channel after the DDP issues an inactivate.

An IAN instruction to receive data should be preceded by a check for channel active and full. This ensures that the DDP has not inactivated the I/O channel because of parity error or abort. If this check is not made, the IAN instruction could hang. †

The time required for the I/O channel to change from active and empty to active and full may vary from 0 to 50 microseconds. Removing the empty check and using the unhangable channel feature of the DCN instruction avoids this delay.

Any of the following will clear out the read ECS condition.

- New function
- PPU or DDP generated inactivate
- Power-on or deadstart master clear
- Master clear port function

READ ECS, 1 REFERENCE - 5X41

The read 1 reference operation is similar to block read ECS, but makes only one ECS reference. This mode takes less time than using the block read mode to do one reference. The read 1 reference terminates when the I/O channel goes inactive.

FUNCTION FLAG REGISTER - 5X01

Using the read ECS function with bit 2^{23} of the ECS address word set causes the DDP to perform function flag register. The function flag register operation allows the DDP to interrogate and/or write into the flag register in the ECS controller. Selecting this mode causes the DDP to send the contents of its address register to the ECS controller, and terminates the read ECS condition within the DDP. The PPS must then inactivate the I/O channel. Selecting and reading status after performing function flag register accomplishes interrogation of the ECS controller flag register. A separate section of this manual describes flag register operations.

---

† If software uses the unhangable channel feature, the PPS may safely inactivate the I/O channel after the DDP issues an inactivate.

WRITE ECS - 5Y02

The block write ECS function causes data to transfer from the PPS to ECS. The DDP responds to a write ECS function by inactivating the I/O channel to which it is connected. The PPS must then activate the I/O channel before it transmits 12-bit data words to the DDP. The initial two 12-bit words transmitted must indicate the address at which the first ECS word will write. The DDP loads the initial two words into a 24-bit address register. The first word loads into the upper 12 bits, and the second word loads into the lower 12 bits.

During a write ECS operation, the DDP assembles eight 60-bit words (one ECS record) before writing into ECS. Each time a full ECS record becomes available, the DDP writes it into ECS and begins to assemble the next record. The address register automatically increments for each 60-bit word written into ECS. Unless an error condition occurs, data transfers in this way until the PPS inactivates the I/O channel to which the DDP is connected. If the DDP has accumulated a partial ECS record when a write operation ends, an inactivate instruction causes the DDP to write the partial record into ECS. If the DDP has assembled less than an integer number of 60-bit words at the end of a write operation, the partial 60-bit word writes into ECS with zeros making up the missing 12-bit words. A partial record writing into ECS does not alter the remaining ECS record. Therefore, a reference of less than one ECS record is possible. When the I/O channel inactivates, the write ECS condition clears out of the DDP. However, completion of a write ECS operation can require up to 50 microseconds after the I/O channel inactivates. Status checking before issuing a new function avoids losing the last ECS record or writing it into the wrong address.

Three error conditions may occur during a write ECS operation: channel parity error, ECS controller parity error, and ECS abort. If it detects an error, the DDP inactivates the I/O channel. The inactivate goes to the I/O channel in place of an empty response to a full signal. This eliminates the possibility of hanging the channel when the PPU inactivates it.†

† If software uses the unhangable channel feature, the PPS may safely inactivate the I/O channel after the DDP issues an inactivate.

The following is an instruction sequence to write ECS.

FNC	5002	ECS block write
OAM	XXXX	Where (A)=2 + the number of 12-bit bytes of data to be sent (first two words comprise the address)
IJM	Error:	Channel inactivated via DDP; read status
DNC	Read Status:	Keeping in mind that the channel must be empty†, check for abort or accept. Continue to read status until one or the other is detected (may take as long as 50 microseconds)

The PPS should inactivate the I/O channel to terminate a write operation only when the channel is empty.

An OAN instruction to transmit data should be preceded by a check for channel active and empty. This ensures that the DDP has not inactivated the I/O channel because of an abort. If this check is not made, the OAN instruction could hang.†

Any of the following will clear out write ECS condition.

- New function - other than status 5004
- DDP generated inactivate
- Power-on or deadstart master clear
- Master clear port function

SELECT STATUS - 5Z04

This function makes the status of a port available to the PPS. The DDP responds to this function by inactivating the I/O channel to which it is connected. The PPS must then activate the channel and receive a 12-bit status word. Issuing another input instruction repeats the status check. The PPS must inactivate the I/O channel to terminate reading status. Bits 2^0 through 2^5 of the status word indicate the following conditions.

† If software uses the unhangable channel feature, the PPS may safely inactivate the I/O channel after the DDP issues an inactivate.

Bit 2^0 — ECS abort indicates that the DDP has received an abort signal from the ECS controller.

Bit 2^1 — ECS accept indicates that the DDP has received an accept signal from the ECS controller.

Bit 2^2 — ECS parity error indicates that the DDP has received an ECS parity error signal from the ECS controller.

Bit 2^3 — ECS write indicates that the DDP port is busy with a write to ECS. This status bit clears when the write operation terminates.

Bit 2^4 — I/O channel parity error indicates that the DDP has received a 12-bit word with incorrect parity from the PPS.

Bit 2^5 — ECS controller parity error indicates that the DDP has detected incorrect parity in data sent to or received from the ECS controller.

Various combinations of status bits indicate the following error conditions.

0020 — Indicates that the DDP has detected a parity error in the address received from the PPS during a read or write ECS operation.

0022 — Indicates that the DDP has detected an error in the data received from the PPS during a write ECS operation.

0041 — Indicates a parity error on the address sent to the ECS controller during a read ECS, write ECS, or function flag register operation.

0042 — Indicates that the DDP has detected a parity error in the data received from the ECS controller during a write or read ECS operation.

0046 — Indicates that the DDP has detected an ECS parity error in the data received from the ECS controller during a read ECS operation.

The following bits in the status word are cleared by a master clear port function, power-on master clear, or the next nonstatus function, after reading status.

Bit 2^0 - ECS abort
Bit 2^1 - ECS accept
Bit 2^2 - ECS parity error
Bit 2^4 - I/O channel parity error
Bit 2^5 - ECS controller parity error

Bit 2^1 is also cleared by a request to ECS. Bit 2^3 clears when the write ECS operation terminates.

Reading status is the only way to clear a DDP generated inactivate due to ECS abort, ECS parity error, ECS controller parity error, or I/O channel parity error. If this is not done, the DDP immediately sends an inactive signal when the PPU activates the I/O channel.

MASTER CLEAR PORT - 5010

This function is programmable clear; it clears only the port to which it is issued.

MAINTENANCE MODE READ - 5Z21

This function causes a DDP port to transmit to a PPS only the data stored in its port buffer register. The DDP does not read ECS in this mode. A port buffer register can store up to 16 60-bit words. These words are disassembled into 12-bit words and transmitted to the PPS to which the port is connected. When used with a maintenance mode write, this function checks out all of a port's data logic without disturbing ECS.

MAINTENANCE MODE WRITE - 5022

This function causes a PPS to transmit data to a port's buffer register. Data does not write into ECS in this mode. The port accepts up to 80 12-bit words, assembles them into 60-bit words, and stores up to 16 60-bit words in the buffer register. If the PPS attempts to send more than 80 12-bit words, the DDP will not respond to the full signal for the 81st word.

INVERT CHANNEL PARITY - 51XX

This function causes data transmitted by the DDP over the I/O channel to go out with even parity.

FUNCTION ECS CONTROLLER TO SEND ZERO PARITY - 5201

This function initiates a read ECS operation, but causes the ECS controller to send a zero parity bit with each 60-bit ECS word. This function is used to check the DDP parity network.

SEND ZERO PARITY TO THE ECS CONTROLLER WITH DATA - 5202

This function initiates a write ECS operation, but causes the DDP to send a zero parity bit with each 60-bit word transmitted to ECS. This function is used to check the data parity network in the ECS controller.

SEND ZERO PARITY TO THE ECS CONTROLLER WITH ADDRESS - 54XX

This function causes the DDP to send a zero parity bit with the address word sent to the ECS controller. This function is used to check the address parity network in the ECS controller.

PROGRAMMING SAMPLES A

BLOCK TRANSFER FROM ECS TO CENTRAL MEMORY

Example: Assume that a program starting at an inbounds address contains a read ECS (011) instruction. The instruction specifies the number of words to be transferred as (Bj) + K. Prior to execution of this instruction, it is assumed that the program loaded registers Bj, A0, and X0 with the control parameters. Because the program was initiated by executing an exchange jump, the central processor holds the reference addresses RAC and RAE, and the field lengths FLC and FLE as part of the exchange jump package.

It is desired, in this example, to transfer a block of 300_8 60-bit words from ECS to central memory. The various control parameters (octal) are assumed to be as follows:

(Bj)	=	100	RAE	=	26500
K	=	200	FLE	=	1300
RAC	=	1400	(A0)	=	4600
FLC	=	5300	(X0)	=	603

A map of central memory and ECS would then appear as indicated in Figure A-1. A similar operation occurs for the write ECS (012) instruction.

For both read and write operations, the parameters held with the central processor which control the block transfer (namely, Bj, X0, A0, RAC, RAE, FLC, and FLE) do not vary during the transfer. Therefore, an exchange jump occurring during a transfer may be initiated. However, when the transfer program is again resumed, the transfer is started with the original parameters, and not from the addresses used just before the interruption in the program.

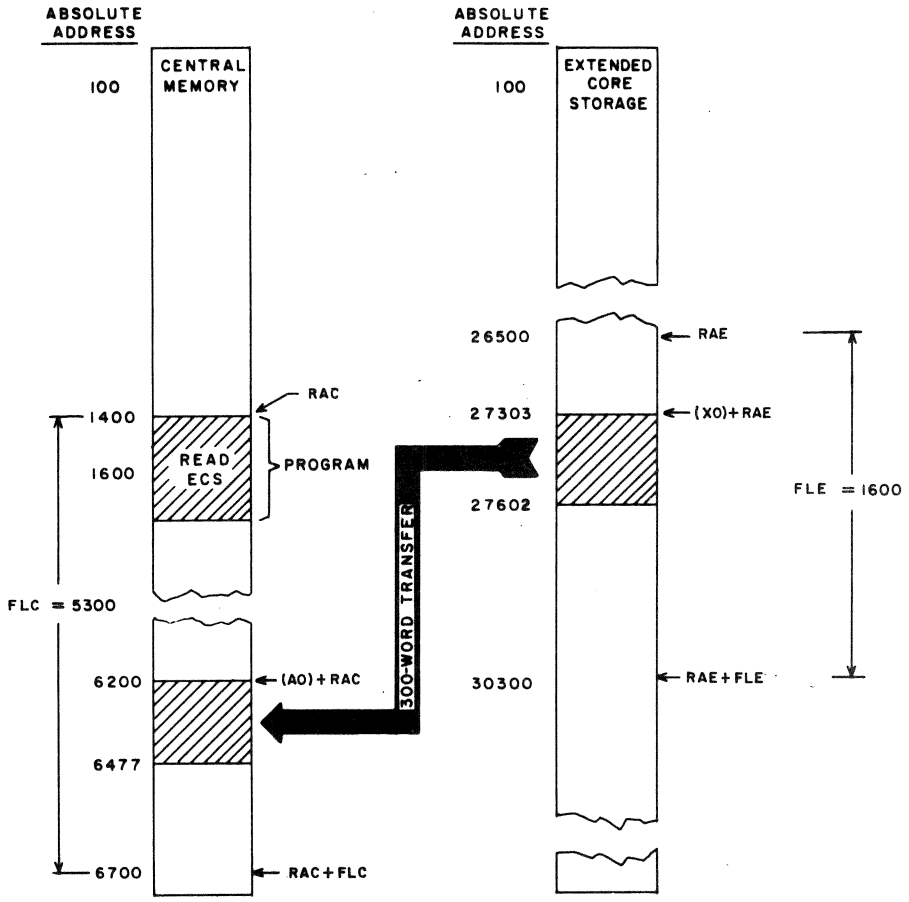


Figure A-1. Memory Map - Read ECS Example

DDP PROGRAMMING SAMPLES

INPUT SEQUENCE

The following is a sample program outline to input ECS data via the DDP.

```
    START
    FNC     5010B     Clear port (not required)
    FNC     5001B     Select ECS read (5041B, if only one ECS reference is desired)
    ACN               Activate channel
    LDN     2         Number of words to be output
    OAM     XXXX      Output address
    LDC     N1        Number of words to be input
    IAM     XXXX      Input data
B   IJM     S         Error; inactivated via DDP read status
    (Jump to D if read, one reference functioned)
    EJM     B         Wait for active and full before inactivating unless read
                      one reference is selected
D   DCN               Inactivate channel
    XXX               Continue program

    Error Routine
S   FNC     5004B     Select status
    ACN               Activate channel
    IAN               Input status word
    Ⓐ
```

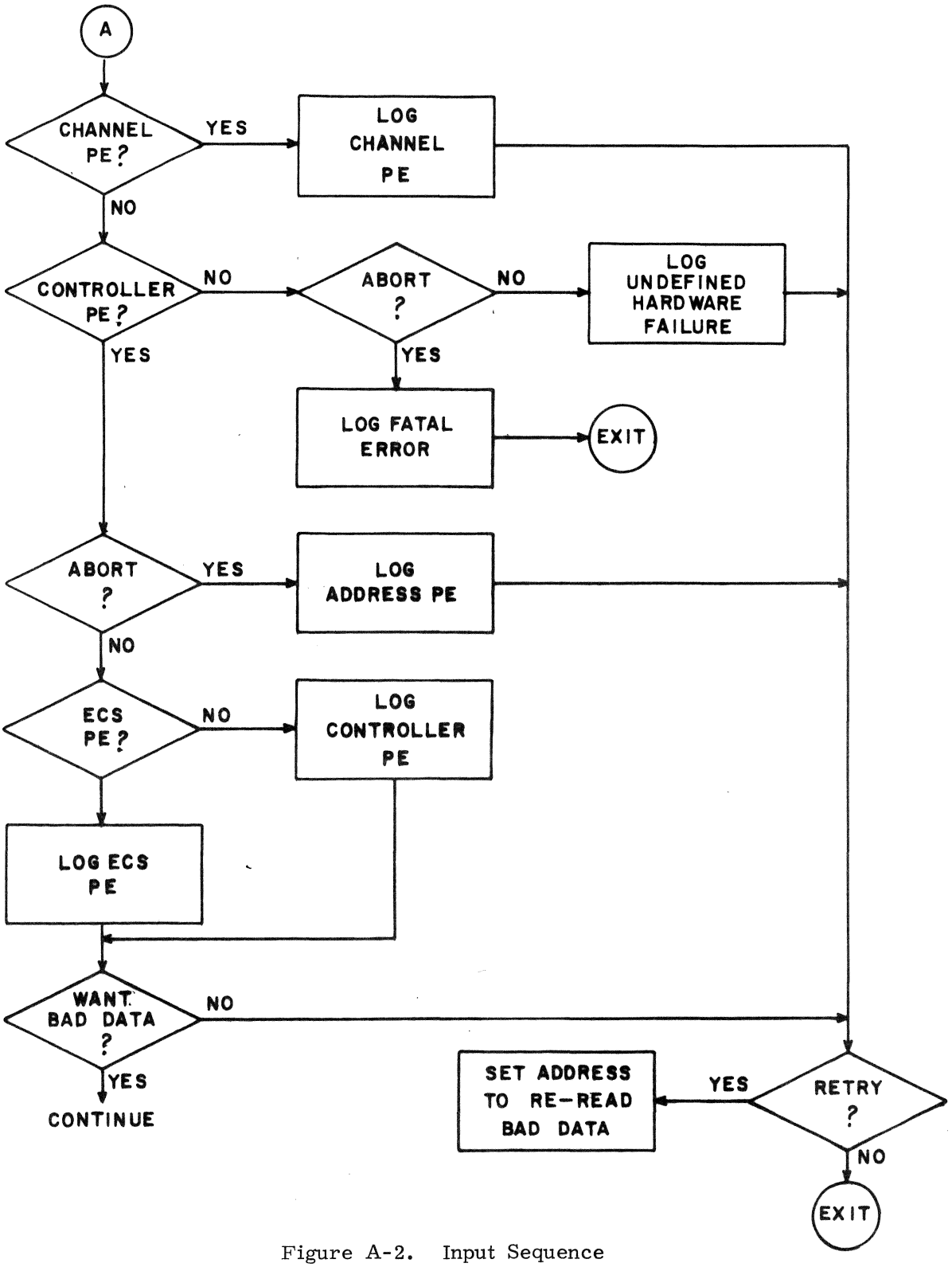


Figure A-2. Input Sequence

```
    DCN             Inactivate data channel
    FCN     5021B   ECS read function, maintenance mode
    ACN             Activate channel
    LDN     2       Number of words to be output.
    OAM     XXXX    Output address - any address will do.
    LDN     N2      Number of words to be input (N2 ≤ 40(10)).
    IAM     XXXX    Input data:  this will input the ECS record which has bad
                    data
    DCN             Inactivate channel
    XXX             Continue
    XXX
C   DCN             Inactivate channel
    FCN     5001B   Function new ECS read
    ACN             Activate channel
    LDN     2
    OAM     XXXX    Output address of word to be read
    LDN     N3
    IAM     XXXX    Input data
    ETC.
```

OUTPUT SEQUENCE

The following is a sample program to output data to ECS via the DDP.

```
    START
A   FNC     5002B   Function ECS write
    ACN             Activate channel
    LDN     2+N     Number of words to be output
    OAM     XXXX    Output address and data
B   IJM     S       Error; inactivated via DDP, read status
    FJM     B       Wait for active and empty before inactivating
    DCN             Inactivate channel
    RJM     Status  Status for end of write and no abort
    XXX             Continue program

    Error Routine
S   FNC     5004B   Select status
    ACN             Activate channel
    IAN     XXXX    Input status word
```

Ⓐ

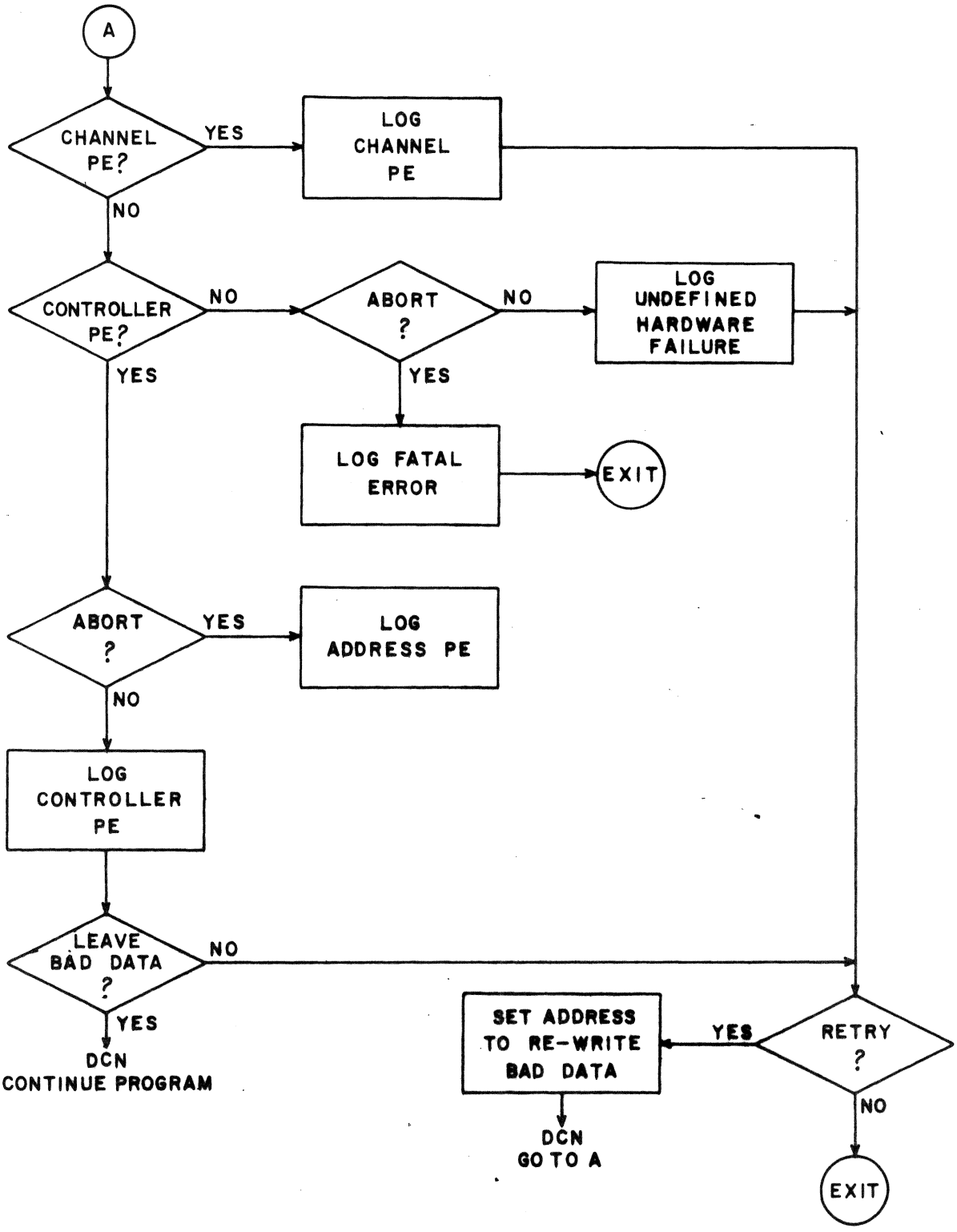


Figure A-3. Output Sequence

FUNCTION FLAG REGISTER SEQUENCE

The following is a sample program to perform a flag register function.

```
START
FNC     5001B    Function ECS read
ACN              Activate channel
LDN     2
OAM     XXXX     Output address, (A) = 2
                 Address = 1XX 000 YYY YYY YYY YYY YYY YYY
                 Where: 1XX determines whether the flag function
                        is ready select, selective set, status,
                        or selective clear.  Y through Y are the
                        flag word bits.
DCN              Inactive channel
FCN     5004B    Select status
ACN              Activate channel
LDN     1
IAM     XXXX     Input status word
```

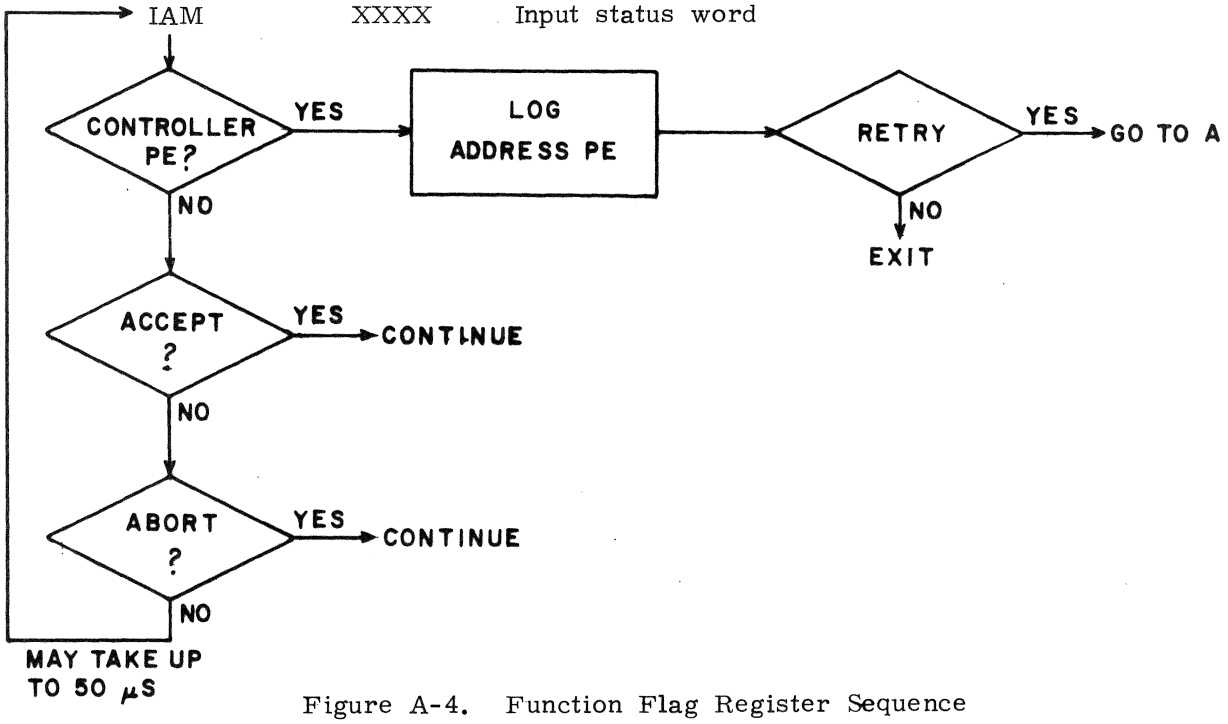


Figure A-4. Function Flag Register Sequence

MASTER CLEAR PORT SEQUENCE

To send out a master clear port:

FNC	5010B	Function master clear port
XXX		Continue

COMMENT SHEET

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ECS Subsystem Hardware Reference Manual

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